IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A system for generating an OVSF code comprising:

a binary counter for providing a binary count comprising a plurality of sequential M-bit binary numbers;

bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit;

an index selector, for providing an M-bit binary identification of said OVSF code; and

a logical reduction means having a first input from the counter and a second input from the index selector and having an output; whereby the desired OVSF code is output from said output.

2. (Currently amended) A code generator for generating individual binary codes of a set of binary codes, each binary code having 2^M ~~bits;~~ bits, the code generator comprising:

a counter having an output and sequentially outputting M-bit counts in a parallel orientation, each successive count being incremented by 1;

bit reordering means, coupled to said output of said counter, for receiving each M-bit count, whereby the M-bit counts are ordered from least significant bit to most significant bit, and whereby said bit reordering means reorders the bits from most significant bit to least significant bit;

an index selector for outputting an M-bit code identifier in a parallel orientation;

a parallel array of M logical gates, each having an output and a first input being one parallel bit from said ~~counter~~ bit ordering means and a second input being one parallel bit from said index selector; and

a reduction network of logical gates associated with the outputs of said parallel array of logical gates for outputting a single code bit each time a parallel M-bit count is input to said parallel logical gate array from said ~~counter~~ bit ordering means, such that the binary code which is identified by the M-bit code identifier is produced after 2^M iterations.

3. (Canceled)

4. (Currently amended) A system for generating a desired pseudorandom code comprising:

a binary counter for providing a plurality of M-bit sequential binary numbers;

bit reordering means for reordering the bits of said binary counter from least significant bit to most significant bit;

an index selector, for outputting an M-bit code identifier of the desired pseudorandom code;

at least M logical gates, each having a first input from ~~the binary counter~~ said bit ordering means and a second input from ~~the~~ said index selector, and each having an output; and

an XOR tree for XORing said outputs of said logical gates to provide an XORed output; whereby the desired pseudorandom code is output from said XORed output.

5. (Canceled)

6. (Currently amended) A code generator for generating an individual binary code from a set of N binary codes, each binary code having M ~~bits;~~ bits, the code generator comprising:

a counter having an output and sequentially outputting M-bit binary numbers, each successive binary number being incremented by 1;

bit reordering means, coupled to said output of said counter, for receiving each M-bit binary number having bits ordered from least significant bit to most significant bit, whereby said bit reordering means reorders the bits from most significant bit to least significant bit;

an index selector for outputting an M-bit code;

a logical gate array having a first input from said ~~counter~~ bit ordering means and a second input from said index selector, and having an output;

a reduction network of logical gates associated with ~~the~~ said output of said logical gate array for outputting a single code bit each time an M-bit binary number is input to said logical gate array from said ~~counter~~ bit ordering means, such that the binary code identified by the M-bit code is produced after 2^M iterations.

7. (Canceled)

8. (Currently amended) The code generator of claim [[7]] 6, further comprising a switch coupled to said bit reordering means, whereby when ~~the~~ said switch is in a first position, ~~the~~ said bit reordering means is coupled to ~~the~~ said output of said counter to reorder the bits of said binary number, and when ~~the~~ said switch is in a second position, ~~the~~ said bit reordering means is decoupled from ~~the~~ said output of said counter and the bits of said binary number are not reordered.

9. - 12. (Canceled)